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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,846	02/25/2004	Qiang Luo	50019.0272US01	2949

1333 7590 07/13/2006

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,846	LUO, QIANG	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/24/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the Amendment of 4/24/06

Drawings

1. The replacement drawings were received on 24 April 2006. These drawings are approved.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim1-7 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2001/0017382 to Rhodes et al. (cited by applicant) in view of U.S. Patent No. 6,639,293 to Furumiya et al.

Regarding claims 1, 5 and 19, Rhodes discloses a method for low dark current imaging, comprising: forming a substrate (100) that may include epitaxial layers of silicon on a base silicon substrate (see paragraph 0023), forming a first well (112, 212) of a first polarity type above the substrate (p-type; paragraph 0025); forming a first oxide layer (120, 220) on the surface of the first well (see figure 7) such that the first oxide layer comprises an opening through which a portion of the first well is exposed (region between the two field oxide portions;

see figures 4 and 7); and forming a diode electrode structure (110 and 130; alternately 230; see figures 6 and 9) of a second polarity type opposite the first polarity type (n-type; paragraphs 0026, 0028; 0043), wherein the diode electrode structure is formed within an area within the exposed portion of the first well (see figures 6 and 9) such that an intervening portion of the first well exists between the diode electrode structure and first oxide layer (see figures 6 and 9; intervening portion is the portion of 112/212 exposed at the surface and between 130/230 and 120/220).

Rhodes fails to directly teach a structure including a heavily doped substrate of a first polarity, a first epitaxial layer of a first polarity on the substrate, and a well of a first polarity over the first layer.

Furumiya teaches that it is advantageous for CMOS image sensors to use a heavily doped substrate of a first polarity type (26), an epitaxial layer of the first polarity type thereon (28), and a well of the first polarity type (27) formed on the epitaxial layer (figure 5; note that the description of epitaxially forming layer 27, and then doping the layer in selected locations would correspond with forming a p-well; see column 7, lines 45-67), rather than using prior art structures employing only a lightly doped substrate with a p-well formed therein (see figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the substrate structure of Rhodes include a heavily doped substrate of a first polarity, an epitaxial layer of a first polarity, and a well of a first polarity formed thereon, as suggested by Furumiya. The rationale is as follows: A person having ordinary skill in the art would have been motivated to employ the layer structure of Furumiya, because Furumiya shows that such a structure advantageously provides a reduction in crosstalk between neighboring

pixels as well as an improvement in image resolution (see Furumiya, column 7, line 20 – column 8, line 21) relative to the prior art substrate structures (as in Rhodes).

Regarding claims 2 and 20, Rhodes discloses that the diode electrode structure may be formed with an arsenic implant (paragraph 0026; 0028).

Regarding claims 3 and 21, Rhodes discloses that the intervening portion of the first well is a continuous area around the diode electrode structure (see paragraphs 0025-0026; 120 surrounds 115; and 130 is disposed in 115 such that it is spaced away from 120).

Regarding claims 4 and 22, Rhodes discloses that the interval between the field oxide and the diode electrode structure is about equal to one depletion region at the operating applied bias (see paragraph 0043), which indicates that a substantial portion of the depletion region does not extend to the first oxide layer.

Regarding claims 6, 7, 23, and 24, Rhodes discloses that the oxide layer is formed using LOCOS or a shallow trench isolation (paragraph 0025).

Response to Arguments

4. Applicant's arguments with respect to claims 1-7 and 19-24 have been considered but are moot in view of the new grounds of rejection.

Insofar as such arguments may apply to the present rejection, the Applicant's arguments are addressed as follows:

The Applicant first argues that Rhodes does not include both an epitaxial layer and a well, since layer 140 cannot be considered the well. The Examiner notes that the "epitaxial layer" used for claim 5 in the previous rejection is based on the statement in paragraph 0023 that

the substrate epitaxial layers of silicon supported by a base semiconductor foundation. Hence, layer 100 was considered to include semiconductor substrates with epitaxial layers formed thereon. Since Rhodes does not supply the doping polarity or levels of the substrate and epitaxial layers, the Furumiya reference is used to supply such teachings.

The Applicant further argues that Rhodes does not teach that a substantial portion of the depletion region does not extend to the first oxide layer. The Examiner disagrees. Since Rhodes directly states that the spacing of regions 130,230 from the oxide region has a magnitude of about one depletion region (see paragraph 0043), the Examiner maintains that a substantial portion of the depletion region must not extend to the first oxide layer.

The Applicant further argues that Rhodes includes patterned p-regions 140 in order to achieve the desired depletion region spacing, whereas the Applicant's invention does not require the presence or patterning of p-wells 140. The Examiner appreciates that omission of p-well patterning would advantageously simplify the fabrication. The claims, however, provide no language precluding the presence of the p-well 140. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,614,744 to Merrill teaches that it is advantageous to include an n-epitaxial layer between a p+ substrate and a p-well of a CMOS image sensor, in order to reduce cross talk between pixels.

U.S. Patent No. 6,259,145 to Connolly et al. discloses a CMOS image sensor structure designed to reduce leakage current.

U.S. Patent No. 6,291,280 to Rhodes indicates that the substrate of a CMOS image sensor may include a heavily p-doped substrate, a p-well, and an additional epitaxial layer between the two (see column 2, line 65 – column 3, line 20).

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Replacement Drawings Approved

7/7/06

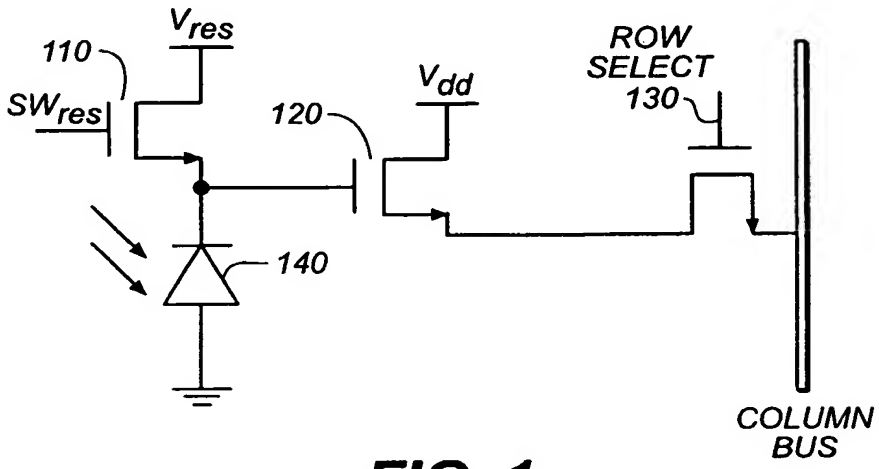

FIG. 1